AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A semiconductor integrated circuit comprising:

a power supply wiring;

a ground wiring; and

a decoupling capacitor formed between said power supply wiring and said ground wiring, said decoupling capacitor having electrodes,

wherein at least one of the electrodes of said decoupling capacitor comprises a shield layer formed in a plane shape on a semiconductor substrate, ~~and~~ said shield layer is connected electrically directly to the semiconductor substrate via a diffusion layer and is fixed to a power supply potential or the ground potential, and all of said decoupling capacitor is located outside of a region overlapping with said diffusion layer.

2. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein, another of the electrodes of said decoupling capacitor, which opposes the electrode comprising said shield layer, includes a wiring layer connected to wirings on an uppermost layer of a multilayer wiring structure via contact electrodes, and a capacitor insulating film for forming said decoupling capacitor is provided between said wiring layer and said shield layer.

3. (currently amended): A semiconductor integrated circuit comprising:

a power supply wiring;

a ground wiring; and

a decoupling circuit formed between said power supply wiring and said ground wiring, said decoupling circuit having electrodes,

wherein at least one electrode of said decoupling circuit comprises a shield layer obtained by covering a plurality of protrusions formed on a semiconductor substrate, ~~and~~ said shield layer is electrically connected directly to the semiconductor substrate via a diffusion layer and is fixed to a power supply potential or the ground potential, and all of said decoupling circuit is located outside of a region overlapping with said diffusion layer.

4. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said protrusions are formed simultaneously with a gate electrode by a same formation process used for the gate electrode.

5. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein said decoupling capacitor is formed on an element isolation oxide film.

6. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein said shield layer comprises a silicon compound of a metal.

7. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said decoupling circuit is formed on an element isolation oxide film.

8. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said shield layer comprises a silicon compound of a metal.

9. (previously presented): The semiconductor integrated circuit as claimed in claim 1, wherein said diffusion layer is a well contact diffusion layer.

10. (previously presented): The semiconductor integrated circuit as claimed in claim 3, wherein said diffusion layer is a well contact diffusion layer.

11. (currently amended): The semiconductor integrated circuit as claimed in claim 1, wherein said semiconductor substrate includes a p-well region and ~~a~~ an n-well region.

12. (currently amended): The semiconductor integrated circuit as claimed in claim 3, wherein said semiconductor substrate includes a p-well region and ~~a~~ an n-well region.